REMARKS

Reconsideration of the above referenced application in view of the enclosed amendments and remarks is requested. This response corrects an informality in the Detailed Description. Claims 1-60 remain pending without amendment. Claims 1, 16, 31, and 46 are the independent claims.

ARGUMENT

The Office Action rejects each of the pending claims based on either 35 U.S.C. § 102(e) or § 103(a).

35 U.S.C. § 102(e)

The Office Action rejects claims 1, 16, 31, and 46 under 35 U.S.C. § 102(e) as being anticipated by U.S. patent no. 6,292,874 to Philip C. Barnett (hereinafter "Barnett"). Applicants respectfully traverse those rejections.

Embodiments of the present invention relate to a processing system with one or more processors, a chipset, storage, a processor nub loader, and a processor nub. The processor nub provides the initial set-up and low-level management of an isolated memory area for the processing system. The processor nub is loaded by the processor nub loader. The processor nub and the processor nub loader may also be referred to as a processor executive (PE) and a PE handler, respectively. (Detailed Description page 11, line 20, through page 13, line 5; and page 14, line 15, through page 18, line 23.)

Specifically, in the present application, claim 1 recites an apparatus with storage to store a "PE handler image to be loaded into the isolated memory area after the chipset is initialized."

By contrast, Barnett relates to a "memory management circuit for a single chip processing circuit, such as a smart card" (col. 2, lines 47-65). Accordingly, Barnett discusses memory management and security in the context of a single chip processing circuit. Unlike the present application, Barnett says nothing about chipsets, processor nubs, or PE handlers.

In the present application, claim 1 not only involves a chipset and a PE handler, but also includes language describing where and when an image for the PE handler is loaded. Barnett clearly does not anticipate an apparatus with storage to store a "PE handler image to be loaded into the isolated memory area after the chipset is initialized." The rejection of claim 1 is therefore improper.

In addition, each of claims 16, 31, and 46 involves features similar to those quoted above with regard to claim 1. For these and other reasons, Barnett does not anticipate claims 1, 16, 31, and 46.

35 U.S.C. § 103(a)

The Office Action rejects claims 2-3, 17-18, 32-33, and 47-48 under 35 U.S.C. § 103(a) as being unpatentable over Barnett, in view of U.S. patent no. 6,035,374 to Ramesh Panwar et al. (hereinafter "Panwar"). Applicants respectfully traverse those rejections.

Panwar relates to a method for "dynamically reconfiguring a processor between uniprocessor and selected multiprocessor configurations" (col. 2, lines 43-48). Neither Panwar nor Barnett provides a motivation to combine Panwar and Barnett.

Additionally, even if Barnett and Panwar were to be combined, the combination would not disclose or suggest all of the features recited in any of claims 2-3, 17-18, 32-33, and 47-48. For instance, claims 2, 17, 32, and 47 involve a thread count indicating the "number of threads currently operating in the isolated execution mode." Neither Barnett nor Panwar disclose the concept of maintaining a count of threads currently operating in a particular mode. Consequently, a combination of Barnett and Panwar would not teach the concept of maintaining a count of the number of threads currently operating in the isolated execution mode.

In addition, since claims 2, 17, 32, and 47 depend from, and therefore implicitly include the features of, claims 1, 16, 31, and 46, respectively, the cited art cannot render the dependent claims obvious unless it discloses or suggests the features of the independent claims. Barnett and Panwar, however, even if combined, do not teach the features discussed above with regard to the § 102(e)

rejections of the independent claims. Like Barnett, Panwar does not disclose or suggest a PE handler image to be loaded into an isolated memory area of a processing system after a chipset for the processing system is initialized.

For the above reasons and other reasons, the rejections of claims 2, 17, 32, and 47 are improper.

Claims 3, 18, 33, and 48 depend from claims 2, 17, 32, and 47, respectively, and therefore also implicitly include the features of the respective ancestor claims. However, as explained above, the cited art does not render the ancestor claims unpatentable. Furthermore, claims 3, 18, 33, and 48 involve identifiers for executive entities such as a PEs "operating in the isolated execution mode," as well as a "lock pattern" that specifies which executive entities executing in the isolated mode are to be locked. As explained in the Detailed Description at page 17, line 22, through page 18, line 2, to be "in lock" means that "the corresponding identifier cannot be modified or written." Neither Barnett nor Panwar disclose the concept of locking identifiers for PEs based on a lock pattern. A combination of Barnett and Panwar likewise would not teach those features. For the above reasons and other reasons, the rejections of claims 3, 18, 33, and 48 are improper.

Also, the Office Action rejects claims 4-14, 19-29, 34-44, and 49-59 as being unpatentable over Barnett, in view of Panwar, and further in view of U.S. patent application publication no. US 2002/0007456 A1 to Marcus Peinado et al. (hereinafter "Peinado"). Applicants respectfully traverse those rejections.

The present application was filed on March 31, 2000. Peinado was filed on June 27, 2001. Peinado therefore does not qualify as prior art under 35 U.S.C. § 103(a). Peinado apparently attempts to claim priority from a provisional application filed March 27, 1999. However, since Peinado was not filed within one year from the filing date of the provisional application, Peinado is not entitled to the filing date of the provisional application under 35 U.S.C. § 119(e). For these and other reasons, the rejections of claims 4-14, 19-29, 34-44, and 49-59 are improper.

Also, the Office Action rejects claims 15, 30, 45, and 60 as being unpatentable over Barnett, in view of Panwar and Peinado, and further in view of

U.S. patent no. 6,507,904 issued to Carl M. Ellison et al. (her inafter "Ellison '904"). Applicants respectfully travers those r jections.

As explained above, Peinado does not qualify as prior art to the present application. In addition, Ellison '904 does not qualify as prior art, since the present application and Ellison '904 were both filed on March 31, 2000. For these and other reasons, the rejections of claims 15, 30, 45, and 60 are improper.

Information Disclosure Statements

The Office Action also includes copies of certain Information Disclosure Statements (IDSs) that were filed for this application. The copies include initials to indicate that the references have been considered. Applicants appreciate the Examiner's consideration of those references. However, the Office Action did not include a copy of one IDS that was submitted electronically on January 22, 2004, nor did it include a copy of another IDS that was mailed to the USPTO on January 26, 2004. Copies of those two IDSs are enclosed herewith, together with copies of an associated acknowledgement receipt and an associated return postcard. Applicants respectfully request confirmation that the references in those two IDSs have been considered.

CONCLUSION

In view of the foregoing, claims 1-60 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (512) 314-0349. Prompt issuance of Notice of Allowance is respectfully requested.

Respectfully submitted,

Dated: 5/7/04

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